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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,223	08/19/2003	Peter Bain	015114-065200US	6465

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EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,223	BAIN, PETER	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6 and 13-20* is/are allowed.

6)☒ Claim(s) *1-3,7-10 and 12* is/are rejected.

7)☒ Claim(s) *4 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,140,596 to Weldon, Jr. (hereafter "Weldon").

Weldon shows (Fig. 2) an encoder for generating a Reed-Solomon error-correcting code with redundancy symbols shifted to the middle of the codeword. As Weldon's Reed-Solomon error-correcting code is a cyclic code that is based on a generator polynomial, Weldon's Reed-Solomon error-correcting code is a form of "cyclical redundancy check" (CRC). Each symbol of Weldon's code has 8 bits, providing a "word," and the connections shown by Weldon (Fig. 2) are 8 bits wide. A first set of GF(2^8) multipliers (245a - 245d) provides a "feedforward circuit" and a second set of GF(2^8) multipliers (240a - 240d) provides a "feedback circuit." The outputs of Weldon's first and second sets of multipliers are coupled to a corresponding plurality of 8-bit XOR gates (230a-230d) serving as a "logic circuit" that is a "summing circuit." The outputs of the plurality of 8-bit XOR gates (230a - 230d) are the codeword after all the data symbols of the "message" R(x) have been input (col. 6, lines 63+), thus "an output of the logic circuit provides the cyclical redundancy check bits."

Weldon further shows (Fig. 4) implementing GF multipliers with look-up table ROM. The ROMs used by Weldon presumably each consist of an address decoder for

receiving address input and coupled to an array for outputting the 8-bit word that is addressed. Each of Weldon's ROM address decoders is seen to provide a "first plurality of logic gates coupled to receive the message" and each of Weldon's ROM arrays is seen to provide a "second plurality of logic gates." As eight logic gates are presumably required in the array to output eight bits for each address, it is apparent that eight gates of the array that correspond to a unique address couple to each output of the address decoder and, accordingly, "at least one of the first plurality of logic gates couple(s) to at least two of the second plurality of logic gates" in each of Weldon's ROMs.

Regarding claim 10, Weldon also shows (Fig. 4) encoder input data registers providing a "plurality of flip-flops coupled to provide outputs to the first plurality of logic gates."

3. Claims 1-3, 7-9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by the published article "High-Speed CRC Computation Using State-Space Transformations" by Derby (hereafter "Derby").

Derby shows (Fig. 3) an M-bit-parallel encoder for generating a "cyclical redundancy check" (CRC). Each "word" input to Derby's decoder is M bits wide. A $\mathbf{B}_{Mt}$ matrix multiplier provides a "feedforward circuit" and an $\mathbf{A}_{Mt}$ matrix multiplier provides a "feedback circuit." A summing node (M-bit XOR) shown by Derby, in combination with a third matrix multiplier $\mathbf{C}_{Mt}$, provides a "logic circuit" that outputs the CRC and comprises a "summing circuit" that uses an "exclusive-or function."

Regarding claims 7-9, Derby's matrix multipliers $\mathbf{B}_{Mt}$ and $\mathbf{A}_{Mt}$ each consist of over four hundred XOR gates, assuming no grouping of logic terms is used (p. 170, col. 1, lines 9+). As understood by the examiner, grouping of logic terms produces intermediate logic terms to be used as input for plural further logic expressions and, accordingly Derby's grouping of logic terms in the matrix multipliers, including the $\mathbf{B}_{Mt}$ "feedforward" multiplier corresponds to a combinational logic having "a first plurality of logic gates ... coupled to receive the message and provide outputs to a second plurality of logic gates" such that "at least one of the first plurality of logic gates couple(s) to at least two of the second plurality of logic gates."

Regarding claims 1 and 12, Derby indicates (p. 170, col. 1, lines 16+) a register, presumably comprising "a plurality of flip-flops," is needed for each bit of the multiplication result generated by each matrix multiplier. Such a multiplier, including the result registers and employing grouping of logic terms, accordingly functions by "logically combining a plurality of the plurality of message bits into a plurality of logic expressions, combining the plurality of logical expressions into a plurality of terms, and storing the plurality of terms." Derby also mentions software implementation of CRC encoding, which indicates the use of processor registers for all intermediate and final results.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weldon.

Weldon doesn't mention storing the "terms" that make up the "feedforward bits" in Weldon's logic, which would be provided by a software implementation of CRC generation. Official Notice is given that providing storage for all intermediate and final results in a software implementation of a logic process was conventional at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Weldon's CRC generation process by using a software-programmed computer, thereby providing storage of the feedforward terms. Such an implementation would have been obvious because the advantages in implementing a logical process by means of a programmed computer were already well known.

6. Claims 1-3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weldon in view of U.S. Patent No. 3,634,883 to Kreidermacher.

Weldon doesn't mention storing the "terms" that make up the "feedforward bits" in Weldon's logic, which would be provided by a software implementation of CRC generation or by, when ROM multipliers are used as suggested by Weldon, a ROM data register. Providing a data register for a ROM in hardware logic was conventional at the time the invention was made, as evidenced by Kreidermacher. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to

implement Weldon's ROM functions using a ROM data register, thereby providing means for storing the feedforward terms. Such an implementation would have been obvious because the usefulness for providing a data register for ROM was already well known.

Allowable Subject Matter

7. Claims 5, 6 and 13-20 are allowed.

8. Claims 4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments with respect to claims 1-3, 7-10 and 12 have been considered but are moot in view of the new grounds of rejection.

Applicant notes that Darby "does not specify what is meant by grouping of terms." Darby states that by proper grouping of terms it is possible to reduce the depth of the XOR trees and the total number of XOR gates. Anyone with a basic understanding of boolean logic should already understand what is meant by "grouping of terms." Every binary input and output value of a logic gate is a "term" and "terms" are "grouped" ("combined") to form a "logical expression" by the operation of the logic gate. In other words, a logic gate performing A XOR B is a gate that "groups" ("combines") term A with term B to form the "logical expression" A XOR B. Certainly it is the case

that the output of any XOR gate is a "logical expression," and certainly it is the case that an XOR tree combines together "logical expressions" output from XOR tree first stage gates and forms a further "term" in the next stage of the tree. Accordingly, combining "message bits" into "logical expressions" and combining "logical expressions" into "terms" requires no more than a pair of two-stage XOR trees arranged in any way.

Applicant's discussion regarding the patent to Weldon is not specific enough to address further.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The cited patents show logic including ROM data registers.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb